PATENT ABSTRACTS OF JAPAN

(11)Publication number : **05-121409**

(43)Date of publication of application : **18.05.1993**

(51)Int.Cl. **H01L 21/321**

(21)Application number : **03-283367**

(22)Date of filing : **30.10.1991**

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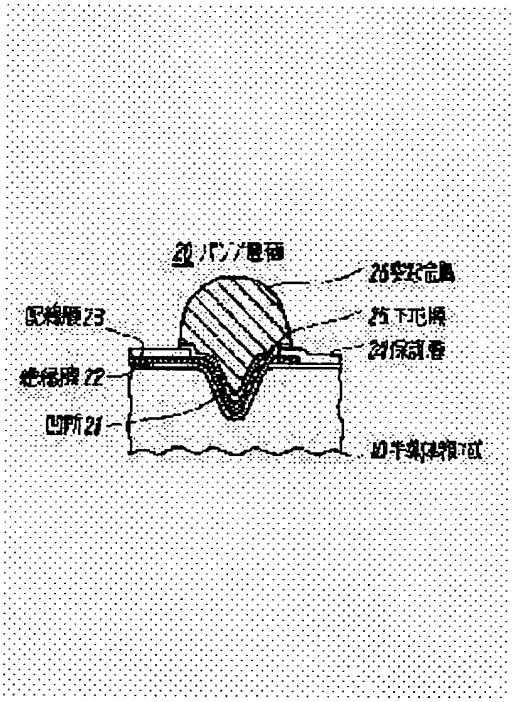
(54) BUMP ELECTRODE FOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:

PURPOSE: To increase attaching strength of a bump electrode which is bumped and fixed to the flip chip for an integrated circuit device even if the bump electrode is miniaturized.

CONSTITUTION: A V-shape recess 21 is provided in a semiconductor area 10 of a chip, and the semiconductor area including the surface is covered with an insulating film 22. On top of that a wiring film 23 of an integrated circuit is laid out. Then, a window is provided on a protecting film 24 covering a chip surface so as to expose the recess 21 and the wiring film 23. The window part is coated with a thin metal base film 25 connected with the wiring film 23. On top of that, a projecting metal 26 for a bump electrode 20 is bumped and fixed by electroplating.



LEGAL STATUS

[Date of request for examination] 23.07.1997

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]

[Date of final disposal for application]

[Patent number] 3077316

[Date of registration] 16.06.2000

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] The bump electrode for integrated circuit devices characterized by providing the following. The hollow dug deep in the shape of V character in the semiconductor region of the bump electrode bottom. It is a wrap insulator layer about the front face of a semiconductor region including this hollow. The wiring film of the metal which was arranged on the insulator layer and connected with the integrated circuit. The salient metal which protruded with electrolysis plating on the thin metaled ground film which was made to expose in an aperture only the predetermined range and hollow of a wiring film in which a bump electrode should be prepared, and was prepared so that the window part of a wrap protective coat and this protective coat might be covered and the front face of an integrated circuit device might be connected with a wiring film, and the ground film.
[Claim 2] The bump electrode for integrated circuit devices characterized by carrying out the depth of a hollow to more than of the same grade with opening width of face in a bump electrode according to claim 1.
[Claim 3] The bump electrode for integrated circuit devices characterized by setting width of face of the root of a salient metal to 30 micrometers or less in a bump electrode according to claim 1.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the small bump electrode or salient electrode which protrudes on the chip in order to connect an integrated circuit device with the exterior.
[0002]
[Description of the Prior Art] Although rationalization of the mounting gestalt at the time of including it in various electronic circuitries and electronic instruments with remarkable progress of the high integration technology of semiconductor integrated circuit equipment in recent years, and the reduction of time and effort and reduction of a space which especially mounting takes have come to be required Mounting with a chip state is more advantageous rather than mounting, after once containing the chip of an integrated circuit device to a plastic package etc. as everyone knows. For this reason, the so-called flip chip which made the above-mentioned bump electrode protrude on the electronic instruments mass-produced has come to be adopted widely. Although it is known well, the conventional typical structure of this bump electrode is explained briefly [below] with reference to drawing 5 .
[0003] Drawing 5 shows the state where the bump electrode 20 of solder protruded on the semiconductor region 10 of the chip of an integrated circuit device, in a cross section. The wiring film 23 of aluminum connected with the integrated circuit made in the semiconductor region 10 is arranged in the insulator layer 22 bottom, such as a wrap silicon oxide, in the front face of a semiconductor region 10, in order to form the bump electrode 20 on the edge, opening of the aperture is carried out for the wiring film 23 to the protective coats 24, such as a wrap silicon nitride, and the wiring film 23 is exposed. After covering this window part first with the ground film 25 of the very thin metal which consists of titanium or copper, the salient metal 26 is grown up into predetermined height by the electrolysis galvanizing method, and it considers as the bump electrode 20 which is made to carry out melting of the solder of the salient metal 26 by short-time heating, and has a radius of circle at a nose of cam in this example.
[0004] In mounting of a flip chip equipped with this bump electrode 20, it places on the mounting other party with the posture which turned the front face to the bottom, for example contrary to drawing 5 , where the nose of cam of the bump electrode 20 is contacted to the other party's conductor, it heats, and soldering junction of the solder of the salient metal 26 is carried out at a conductor. Since the fixation and connection to the mounting other party of a flip chip are simultaneously achieved by this, the time and effort which mounting work takes can be saved, and a mounting space can be reduced to the minimum.
[0005]
[Problem(s) to be Solved by the Invention] By the way, while the chip size of an integrated circuit device is reduced by progress of high integration, it is in the inclination which the number of circuits incorporated in a chip also increases, and the number of external nodes increases, and in a certain kind of integrated circuit device, the need of arranging hundreds of bump electrodes in several mm chip of an angle came out. For this reason, the former Although it is necessary to set to 30 micrometers or less size

of the bump electrode which was about 100-micrometer a path or an angle, when it miniaturizes, there is a problem to the chip of a root to which it attaches in or a bonding strength falls.
[0006] That is, it becomes easy to exfoliate by the slight external force which an actual bonding strength falls further since the reliability of both the film adhesion that the area of the root will drop to about 1/10 if the bump electrode of the diameter of 100micrometer is set to 30 micrometers, intensity falls by 1 figure only by it, and also are between the salient metal 20 of drawing 5 and a semiconductor region 10 falls, and is applied at the time of mounting etc. simply.
[0007] Thus, since strengthening of the intensity of the root of a bump electrode is high integration of an integrated circuit device with many external connection, this invention aims at raising the installation intensity to the semiconductor chip of a bump electrode from a required situation.
[0008]
[Means for Solving the Problem] In the bump electrode by this invention, a hollow is dug deep in the shape of V character in the semiconductor region of the bottom. Are wearing the front face of a semiconductor region including this hollow by the insulator layer, and the wiring film of the metal connected with the integrated circuit on the insulator layer is arranged. Only the connection place and hollow with the exterior of a wiring film are exposed in an aperture, and the front face of an integrated circuit device is worn by the protective coat, it covers by the ground film of a thin metal so that the window part of this protective coat may be connected with a wiring film, and the above-mentioned purpose is attained by protruding a salient metal with electrolysis plating on a ground film.
[0009] In addition, the depth of the hollow of the shape of V above-mentioned character is desirable when carrying out to more than of the same grade with the opening width of face raises the installation intensity of a bump electrode. Sufficient effect which usually raises installation intensity because the effective-area product of this hollow carries out to 25% or more of the area of the root of a bump electrode is acquired. Moreover, when a bump electrode is especially small, it is advantageous to consider as the structure which excluded the wiring film in a hollow. As for the bump electrode by this this invention, it is advantageous especially to apply, when the root width of face is 30 micrometers or less as mentioned above.
[0010]
[Function] Since it depends for this invention on the adhesion in the flat side of the film which has the installation intensity to the semiconductor region of the salient metal of the conventional bump electrode among both, It is what noted that the cause of the problem was in the point which the exfoliation force commits chiefly to this flat faying surface when especially external force is received in a longitudinal direction. By protruding a salient metal on the hollow dug deep in the shape of V character in the semiconductor region so that it might say the composition of the preceding clause It succeeds in raising 1 or more figures of intensity of the root of a bump electrode conventionally by making it compressive force surely applied the film of the bottom, and between films by everything but the exfoliation force, when lateral external force is applied to a salient metal, and extending the area of a faying surface or the acceptance side of external force by the hollow.
[0011] That is, since above-mentioned compressive force mainly works as the reaction force to the angular-moment force applied to a salient metal by longitudinal direction external force, the reaction force by the exfoliation force is very slight and it ends, in the bump electrode of this invention, the intensity to exfoliation of the root can be improved sharply. Moreover, although a lengthwise pressure is applied to a salient metal, of course at the time of mounting of a flip chip, since the area of the acceptance side over it spreads by the hollow as mentioned above, the intensity of the root of a bump electrode to this lengthwise external force also improves conventionally.
[0012]
[Example] Hereafter, the example of this invention is explained with reference to drawing. Since the same sign is given to the portion corresponding to [are a different cross section of an example of the bump electrode of this invention, and] these drawing 5 by the cross section corresponding to drawing 5 of the former [drawing 1] of the example of the bump electrode of this invention, the cross section with which drawing 2 illustrates the manufacture method, the important section expanded sectional view of

the chip of an integrated circuit device in which drawing 3 shows the example of application, and drawing 4 , explanation of a duplication portion is given to omit suitably.

[0013] In the example of drawing 1 , solder is used for the salient metal 26 of the bump electrode 20, and, as for the size, height is set to 20-25 micrometers at the root at the diameter of 25-30 micrometer, or an angle. A different point from conventional drawing 5 is that a hollow 21 is dug deep in the shape of V character like illustration in a semiconductor region 10, and the salient metal 26 of the bump electrode 20 protrudes on it. It is good that this hollow 21 is of the same grade as the path of opening or width of face in 25% or more of the root area of the salient metal 60, or digs the area of opening of the upper part deep for the depth to it at large ** a little, for example, the diameter of 15-20 micrometer or an angle, and the depth are set to 15-25 micrometers for up opening in this example.

[0014] Opening of the aperture is carried out so that the wiring film 23 may be exposed in the range which the structure of the bump electrode 20 except this hollow 21 is the same as usual, the front face of a semiconductor region 10 is being worn by the insulator layer 22 including the front face of a hollow 21, it is arranged, including the inside of a hollow 21 at the example of illustration of the metaled wiring film 23 on it, and a protective coat 24 is further put on it, and should form the bump electrode 20. It is prepared so that the ground film 25 of a thin metal may connect with the wiring film 23 within this aperture, and the salient metal 26 of solder protrudes with electrolysis plating on it.

[0015] Subsequently, the point which makes the bump electrode 20 of the structure of drawing 1 with reference to drawing 2 is explained. Drawing 2 (a) The state where the hollow 21 was dug deep from the front face of a semiconductor region 10 is shown. It is good to use the plasma etching method and the reactive-ion-etching method for this hollow 21 digging deep, and it contains oxygen as reactant gas. CF4 and SF6 A hollow 21 can be deeply dug deep in the side configuration of the shape of V exact character of a strong inclination by setting gas pressure and plasma power as anisotropic etching conditions using mixed gas. in addition, this hollow 21 -- digging deep -- before making an integrated circuit to a semiconductor region 10, it is desirable to carry out beforehand and to place

[0016] Drawing 2 (b) It is usually the insulator layer 22 of a silicon oxide to the front face of a semiconductor region 1 first 1-1.5 It attaches by mum thickness and is on the front face. 0.5-1.5 The wiring film 23 of the aluminum of the thickness of mum is arranged by the predetermined circuit pattern. Subsequently, the edge of the wiring film 23 which forms the protective coats 24, such as a silicon nitride, by CVD to 1-2-micrometer thickness, carries out opening of the aperture 24a to this by the dry etching method, and includes the inside of a hollow 21 is exposed, and it considers as the state of illustration. Drawing 2 (c) The state where the ground film 25 was formed on the whole surface is shown. Like usually, this ground film 25 is used as a two-layer film, and titanium as bottom ground film 25a in this example 0.2-0.5 To the thickness of mum Copper is 1-1.5 as top ground film 25b. Membranes are formed by the thickness of mum by the spatter, respectively.

[0017] drawing -- (d) The state where the salient metal 26 was protruded with electrolysis plating is shown. After carrying out patterning of the top ground film 25b of the ground film 25 to the salient metals 26 by photo etching first, the aperture in which the spin coat of the photoresist film 30 is carried out, and only top ground film 25b is exposed according to a photograph process breaks, and it makes grow up alternatively on top ground film 25b like illustration of the salient metal 26 with the electrolysis plating which uses this photoresist film 30 as a mask film, and makes bottom ground film 25a the plating electrode layer of a negative side It considers as the state which a radius of circle is given at the nose of cam, and shows in drawing 1 by removing the photoresist film 30, and etching removing bottom ground film 25a except for the bottom portion of top ground film 25b henceforth, and fusing the salient metal 26 by short-time heating as mentioned above.

[0018] thus, even when small, the intensity of the root to the external force concerning in-every-direction both directions can be high 1 or more figures as mentioned above than before, can boil markedly the trouble which exfoliates by the pressure and shock it is easy to be shocked at the time of transportation of a chip, and mounting, or receives an injury, and can make it decrease in the bump electrode 20 of the structure of drawing 1 which protrudes on the chip of an integrated circuit device Moreover, drawing 2 (d) An electrolysis plater is set behind and it is the etch residue of bottom ground

film 25a 100 kg/cm2 In the result of the experiment removed by the high-pressure jet stream, in spite of having applied the remarkable pressure to the salient metal 26 at the longitudinal direction, it is proved that there is no ablation of the bump electrode 20 almost.

[0019] the example of application which included the bump electrode 20 of drawing 1 in drawing 3 at the integrated circuit device -- the -- an enlarged section shows a part The semiconductor region 10 of the wafer in this example of application is what diffused the junction isolation layer 13 of p form in the periphery section of each chip which an epitaxial layer 12 should be grown up with n form, and should form the bump electrode 20 on the substrate 11 of p form. In the surface section of an epitaxial layer 12, the p form layer 14 and the n form layer 15 for integrated circuits are spread, as shown in drawing, and the wiring film 23 arranged on the insulator layer 22 is connected with the p form layer 14. Although the bump electrode 20 linked to this wiring film 23 is made into narrow root width of face of about 30 micrometers stated to the cross direction of drawing that it can arrange in the narrowest possible pitch by drawing 1 , in this example of application, in order to raise current capacity, it is formed in the longitudinal direction of a view at large root width of face of 60 micrometers, and, for this reason, a hollow 21 is also dug deep by the longitudinal direction of drawing in the shape of [of a little long and slender rectangle cross section] V character.

[0020] In addition, although an integrated circuit device is examined after wafer process killing like usually, since it will become difficult to contact the needle of the probe for an examination if the bump electrode 20 is miniaturized below in the diameter grade of 50 micrometer by this invention, in the example of application of this drawing 3 , the connection pad 40 for an examination connected with the bump electrode 20 is formed. In case this connection pad 40 isolates a wafer for a chip, it is made from the size of quite larger **, for example, 80-micrometer angle, than the bump electrode 20 using the so-called area of the scribe zone for carrying out a scribe. For this reason, the edge of the wiring film 23 is bulged, this is exposed in the aperture which ended in the protective coat 24, and it considers as the connection pad 40.

[0021] A cross section shows the example which is suitable for drawing 4 miniaturizing further the bump electrode 20 of small current capacity using gold or copper rather than the case of drawing 1 to the salient metal 26. Since the opening width of face of a hollow 21 is set to 10-15 micrometers when setting width of face of the root of this bump electrode 20 to about 20 micrometers, in the example of this drawing 4 , the wiring film 23 in a hollow 21 is excluded, and it is arranged only around it. The ground film 25 is formed also in a hollow 21 so that it may connect with this wiring film 23, of course, and gold and copper for salient metal 26 grow by the electrolysis galvanizing method on it. The salient metal 26 becomes the form where it was firmly planted so to speak in the hollow 21, and the high installation intensity to a semiconductor region 10 is obtained by this. In addition, PARAJUUMU etc. is used for the top ground film in the ground film 21 in the case of this example, and the thickness is thinner than the case of drawing 1 . 0.4-0.6 Considering as mum grade is good. The structure of the example of this drawing 3 is advantageous when making the bump electrode 20 into the size of about 20 micrometers or less.

[0022]

[Effect of the Invention] In the bump electrode by this invention, a hollow is dug deep in the shape of V character in the semiconductor region of the bottom as above. Are wearing the front face of a semiconductor region including this hollow by the insulator layer, and the wiring film of the metal connected with the integrated circuit on it is arranged. Since expose the external connection place and hollow in an aperture, and the front face of an integrated circuit device is worn by the protective coat, it covers by the ground film of a thin metal so that a window part may be connected with a wiring film, and the salient metal was made to protrude by the electrolysis galvanizing method on a ground film When especially external force is applied to a salient metal at a longitudinal direction, the compressive force other than the ablation force is surely applied the film of the bottom, and between films. And the area of a faying surface or the acceptance side of external force spreads, the root intensity of a bump electrode improves by 1 or more figures conventionally, and root intensity of the part in which the area of a peach acceptance side spreads to lengthwise external force improves.

[0023] offer of an integrated circuit device with an effect especially apply this invention to the small bump electrode for flip chips with many external nodes, and high [this invention] and the high degree of integration which made it possible to raise the installation intensity to the chip of the bump electrode which was **** on high integration from the former, and to reduce the size of the root to 30 micrometers or less, and arranged hundreds of bump electrodes for the small chip of several mm angle is enabled -- it is .

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TECHNICAL FIELD

[Industrial Application] this invention relates to the small bump electrode or salient electrode which protrudes on the chip in order to connect an integrated circuit device with the exterior.

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PRIOR ART

[Description of the Prior Art] Although rationalization of the mounting gestalt at the time of including it in various electronic circuitries and electronic instruments with remarkable progress of the high integration technology of semiconductor integrated circuit equipment in recent years, and the reduction of time and effort and reduction of a space which especially mounting takes have come to be required Mounting with a chip state is more advantageous rather than mounting, after once containing the chip of an integrated circuit device to a plastic package etc. as everyone knows. For this reason, the so-called flip chip which made the above-mentioned bump electrode protrude on the electronic instruments mass-produced has come to be adopted widely. Although it is known well, the conventional typical structure of this bump electrode is explained briefly [below] with reference to drawing 5 .
[0003] Drawing 5 shows the state where the bump electrode 20 of solder protruded on the semiconductor region 10 of the chip of an integrated circuit device, in a cross section. The wiring film 23 of aluminum connected with the integrated circuit made in the semiconductor region 10 is arranged in the insulator layer 22 bottom, such as a wrap silicon oxide, in the front face of a semiconductor region 10, in order to form the bump electrode 20 on the edge, opening of the aperture is carried out for the wiring film 23 to the protective coats 24, such as a wrap silicon nitride, and the wiring film 23 is exposed. After covering this window part first with the ground film 25 of the very thin metal which consists of titanium or copper, the salient metal 26 is grown up into predetermined height by the electrolysis galvanizing method, and it considers as the bump electrode 20 which is made to carry out melting of the solder of the salient metal 26 by short-time heating, and has a radius of circle at a nose of cam in this example.
[0004] In mounting of a flip chip equipped with this bump electrode 20, it places on the mounting other party with the posture which turned the front face to the bottom, for example contrary to drawing 5 , where the nose of cam of the bump electrode 20 is contacted to the other party's conductor, it heats, and soldering junction of the solder of the salient metal 26 is carried out at a conductor. Since the fixation and connection to the mounting other party of a flip chip are simultaneously achieved by this, the time and effort which mounting work takes can be saved, and a mounting space can be reduced to the minimum.

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EFFECT OF THE INVENTION

[Effect of the Invention] In the bump electrode by this invention, a hollow is dug deep in the shape of V character in the semiconductor region of the bottom as above. Are wearing the front face of a semiconductor region including this hollow by the insulator layer, and the wiring film of the metal connected with the integrated circuit on it is arranged. Since expose the external connection place and hollow in an aperture, and the front face of an integrated circuit device is worn by the protective coat, it covers by the ground film of a thin metal so that a window part may be connected with a wiring film, and the salient metal was made to protrude by the electrolysis galvanizing method on a ground film. When especially external force is applied to a salient metal at a longitudinal direction, the compressive force other than the ablation force is surely applied the film of the bottom, and between films, and the area of a faying surface or the acceptance side of external force spreads, the root intensity of a bump electrode improves by 1 or more figures conventionally, and root intensity of the part in which the area of a peach acceptance side spreads to lengthwise external force improves.
[0023] offer of an integrated circuit device with an effect especially apply this invention to the small bump electrode for flip chips with many external nodes, and high [this invention] and the high degree of integration which made it possible to raise the installation intensity to the chip of the bump electrode which was **** on high integration from the former, and to reduce the size of the root to 30 micrometers or less, and arranged hundreds of bump electrodes for the small chip of several mm angle is enabled -- it is .

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, while the chip size of an integrated circuit device is reduced by progress of high integration, it is in the inclination which the number of circuits incorporated in a chip also increases, and the number of external nodes increases, and in a certain kind of integrated circuit device, the need of arranging hundreds of bump electrodes in several mm chip of an angle came out. For this reason, the former Although it is necessary to set to 30 micrometers or less size of the bump electrode which was about 100-micrometer a path or an angle, when it miniaturizes, there is a problem to the chip of a root to which it attaches in or a bonding strength falls.
[0006] That is, it becomes easy to exfoliate by the slight external force which an actual bonding strength falls further since the reliability of both the film adhesion that the area of the root will drop to about 1/10 if the bump electrode of the diameter of 100micrometer is set to 30 micrometers, intensity falls by 1 figure only by it, and also are between the salient metal 20 of drawing 5 and a semiconductor region 10 falls, and is applied at the time of mounting etc. simply.
[0007] Thus, since strengthening of the intensity of the root of a bump electrode is high integration of an integrated circuit device with many external connection, this invention aims at raising the installation intensity to the semiconductor chip of a bump electrode from a required situation.

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MEANS

[Means for Solving the Problem] In the bump electrode by this invention, a hollow is dug deep in the shape of V character in the semiconductor region of the bottom. Are wearing the front face of a semiconductor region including this hollow by the insulator layer, and the wiring film of the metal connected with the integrated circuit on the insulator layer is arranged. Only the connection place and hollow with the exterior of a wiring film are exposed in an aperture, and the front face of an integrated circuit device is worn by the protective coat, it covers by the ground film of a thin metal so that the window part of this protective coat may be connected with a wiring film, and the above-mentioned purpose is attained by protruding a salient metal with electrolysis plating on a ground film.
[0009] In addition, the depth of the hollow of the shape of V above-mentioned character is desirable when carrying out to more than of the same grade with the opening width of face raises the installation intensity of a bump electrode. Sufficient effect which usually raises installation intensity because the effective-area product of this hollow carries out to 25% or more of the area of the root of a bump electrode is acquired. Moreover, when a bump electrode is especially small, it is advantageous to consider as the structure which excluded the wiring film in a hollow. As for the bump electrode by this this invention, it is advantageous especially to apply, when the root width of face is 30 micrometers or less as mentioned above.

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OPERATION

[Function] In this invention, since it depended on the adhesion in the flat side of the film which has the installation intensity to the semiconductor region of the salient metal of the conventional bump electrode among both, when especially external force was received in a longitudinal direction, it noted that the cause of the problem was in the point which the exfoliation force commits chiefly to this flat faying surface. Therefore, by protruding a salient metal on the hollow dug deep in the shape of V character in the semiconductor region so that it might say the composition of the preceding clause It succeeds in raising 1 or more figures of intensity of the root of a bump electrode conventionally by making it compressive force surely applied the film of the bottom, and between films by everything but the ablation force, when lateral external force is applied to a salient metal, and extending the area of a faying surface or the acceptance side of external force by the hollow.
[0011] That is, since above-mentioned compressive force mainly works as the reaction force to the angular-moment force applied to a salient metal by longitudinal direction external force, the reaction force by the exfoliation force is very slight and it ends, in the bump electrode of this invention, the intensity to exfoliation of the root can be improved sharply. Moreover, although a lengthwise pressure is applied to a salient metal, of course at the time of mounting of a flip chip, since the area of the acceptance side over it spreads by the hollow as mentioned above, the intensity of the root of a bump electrode to this lengthwise external force also improves conventionally.

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EXAMPLE

[Example] Hereafter, the example of this invention is explained with reference to drawing. Since the same sign is given to the portion corresponding to [are a different cross section of an example of the bump electrode of this invention, and] these drawing 5 by the cross section corresponding to drawing 5 of the former [drawing 1] of the example of the bump electrode of this invention, the cross section with which drawing 2 illustrates the manufacture method, the important section expanded sectional view of the chip of an integrated circuit device in which drawing 3 shows the example of application, and drawing 4 , explanation of a duplication portion is given to omit suitably.
[0013] In the example of drawing 1 , solder is used for the salient metal 26 of the bump electrode 20, and, as for the size, height is set to 20-25 micrometers at the root at the diameter of 25-30 micrometer, or an angle. A different point from conventional drawing 5 is that a hollow 21 is dug deep in the shape of V character like illustration in a semiconductor region 10, and the salient metal 26 of the bump electrode 20 protrudes on it. It is good that this hollow 21 is of the same grade as the path of opening or width of face in 25% or more of the root area of the salient metal 60, or digs the area of opening of the upper part deep for the depth to it at large ** a little, for example, the diameter of 15-20 micrometer or an angle, and the depth are set to 15-25 micrometers for up opening in this example.
[0014] Opening of the aperture is carried out so that the wiring film 23 may be exposed in the range which the structure of the bump electrode 20 except this hollow 21 is the same as usual, the front face of a semiconductor region 10 is being worn by the insulator layer 22 including the front face of a hollow 21, it is arranged, including the inside of a hollow 21 at the example of illustration of the metaled wiring film 23 on it, and a protective coat 24 is further put on it, and should form the bump electrode 20. It is prepared so that the ground film 25 of a thin metal may connect with the wiring film 23 within this aperture, and the salient metal 26 of solder protrudes with electrolysis plating on it.
[0015] Subsequently, the point which makes the bump electrode 20 of the structure of drawing 1 with reference to drawing 2 is explained. Drawing 2 (a) The state where the hollow 21 was dug deep from the front face of a semiconductor region 10 is shown. It is good to use the plasma etching method and the reactive-ion-etching method for this hollow 21 digging deep, and it contains oxygen as reactant gas. CF4 and SF6 A hollow 21 can be deeply dug deep in the side configuration of the shape of V exact character of a strong inclination by setting gas pressure and plasma power as anisotropic etching conditions using mixed gas. in addition, this hollow 21 -- digging deep -- before making an integrated circuit to a semiconductor region 10, it is desirable to carry out beforehand and to place
[0016] Drawing 2 (b) It is usually the insulator layer 22 of a silicon oxide to the front face of a semiconductor region 1 first 1-1.5 It attaches by mum thickness and is on the front face. 0.5-1.5 The wiring film 23 of the aluminum of the thickness of mum is arranged by the predetermined circuit pattern. Subsequently, the edge of the wiring film 23 which forms the protective coats 24, such as a silicon nitride, by CVD to 1-2-micrometer thickness, carries out opening of the aperture 24a to this by the dry etching method, and includes the inside of a hollow 21 is exposed, and it considers as the state of illustration. Drawing 2 (c) The state where the ground film 25 was formed on the whole surface is shown. Like usually, this ground film 25 is used as a two-layer film, and titanium as bottom ground film

25a in this example 0.2-0.5 To the thickness of mum Copper is 1-1.5 as top ground film 25b. Membranes are formed by the thickness of mum by the spatter, respectively.
[0017] drawing -- (d) The state where the salient metal 26 was protruded with electrolysis plating is shown. After carrying out patterning of the top ground film 25b of the ground film 25 to the salient metals 26 by photo etching first, the aperture in which the spin coat of the photoresist film 30 is carried out, and only top ground film 25b is exposed according to a photograph process breaks, and it makes grow up alternatively on top ground film 25b like illustration of the salient metal 26 with the electrolysis plating which uses this photoresist film 30 as a mask film, and makes bottom ground film 25a the plating electrode layer of a negative side It considers as the state which a radius of circle is given at the nose of cam, and shows in drawing 1 by removing the photoresist film 30, and etching removing bottom ground film 25a except for the bottom portion of top ground film 25b henceforth, and fusing the salient metal 26 by short-time heating as mentioned above.
[0018] thus, even when small, the intensity of the root to the external force concerning in-every-direction both directions can be high 1 or more figures as mentioned above than before, can boil markedly the trouble which exfoliates by the pressure and shock it is easy to be shocked at the time of transportation of a chip, and mounting, or receives damage, and can make it decrease in the bump electrode 20 of the structure of drawing 1 which protrudes on the chip of an integrated circuit device Moreover, drawing 2 (d) An electrolysis plater is set behind and it is the etch residue of bottom ground film 25a 100 kg/cm2 In the result of the experiment removed by the high-pressure jet stream, in spite of having applied the remarkable pressure to the salient metal 26 at the longitudinal direction, it is proved that there is no exfoliation of the bump electrode 20 almost.
[0019] the example of application which included the bump electrode 20 of drawing 1 in drawing 3 at the integrated circuit device -- the -- an enlarged section shows a part The semiconductor region 10 of the wafer in this example of application is what diffused the junction isolation layer 13 of p form in the periphery section of each chip which an epitaxial layer 12 should be grown up with n form, and should form the bump electrode 20 on the substrate 11 of p form. In the surface section of an epitaxial layer 12, the p form layer 14 and the n form layer 15 for integrated circuits are spread, as shown in drawing, and the wiring film 23 arranged on the insulator layer 22 is connected with the p form layer 14. Although the bump electrode 20 linked to this wiring film 23 is made into narrow root width of face of about 30 micrometers stated to the cross direction of drawing that it can arrange in the narrowest possible pitch by drawing 1 , in this example of application, in order to raise current capacity, it is formed in the longitudinal direction of a view at latus root width of face of 60 micrometers, and, for this reason, a hollow 21 is also dug deep by the longitudinal direction of drawing in the shape of [of a little long and slender rectangle cross section] V character.
[0020] In addition, although an integrated circuit device is examined after wafer process killing like usually, since it will become difficult to contact the needle of the probe for an examination if the bump electrode 20 is miniaturized below in the diameter grade of 50 micrometer by this invention, in the example of application of this drawing 3 , the connection pad 40 for an examination connected with the bump electrode 20 is formed. In case this connection pad 40 isolates a wafer for a chip, it is made from the size of quite larger **, for example, 80-micrometer angle, than the bump electrode 20 using the so-called area of the scribe zone for carrying out a scribe. For this reason, the edge of the wiring film 23 is bulged, this is exposed in the aperture which ended in the protective coat 24, and it considers as the connection pad 40.
[0021] A cross section shows the example which is suitable for drawing 4 miniaturizing further the bump electrode 20 of small current capacity using gold or copper rather than the case of drawing 1 to the salient metal 26. Since the opening width of face of a hollow 21 is set to 10-15 micrometers when setting width of face of the root of this bump electrode 20 to about 20 micrometers, in the example of this drawing 4 , the wiring film 23 in a hollow 21 is excluded, and it is arranged only around it. The ground film 25 is formed also in a hollow 21 so that it may connect with this wiring film 23, of course, and gold and copper for salient metal 26 grow by the electrolysis galvanizing method on it. The salient metal 26 becomes the form where it was firmly planted so to speak in the hollow 21, and the high

installation intensity to a semiconductor region 10 is obtained by this. In addition, PARAJUUMU etc. is used for the top ground film in the ground film 21 in the case of this example, and the thickness is thinner than the case of drawing 1 . 0.4-0.6 Considering as mum grade is good. The structure of the example of this drawing 3 is advantageous when making the bump electrode 20 into the size of about 20 micrometers or less.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section of the example of the bump electrode of this invention.
[Drawing 2] It is the cross section which illustrates the manufacture method of the bump electrode of drawing 1 , and is this drawing (a). A hollow digs deep and they are a next state and this drawing (b). The state before covering of a ground film, and this drawing (c) The state after covering of a ground film, and this drawing (d) The state after the electrolysis plating of a salient metal is shown, respectively.

[Drawing 3] It is the important section expanded sectional view of a flip chip showing the example of application to the integrated circuit device of the bump electrode of drawing 1 .
[Drawing 4] It is the cross section of an example with which the bump electrodes of this invention differ.
[Drawing 5] It is the cross section of the conventional bump electrode.
[Description of Notations]
10 Chip of Integrated Circuit Device, or Semiconductor Region of Wafer
20 Bump Electrode
21 Hollow
22 Insulator Layer
23 Wiring Film
24 Protective Coat
25 Ground Film
25a Bottom ground film
25b Top ground film
26 Salient Metal
30 Photoresist Film as a Mask for Electrolysis Plating

[Translation done.]

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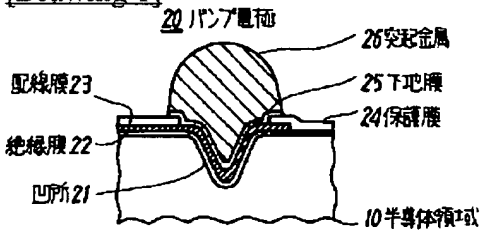
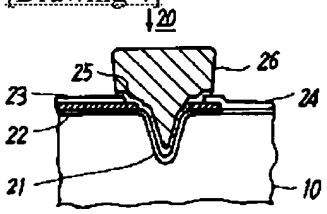
DRAWINGS

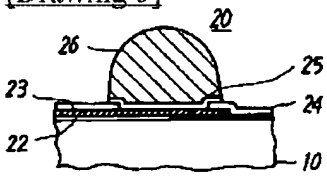
[Drawing 1]



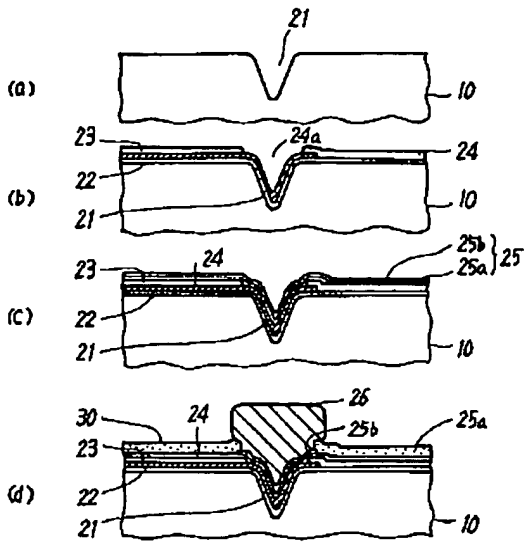
[Drawing 4]



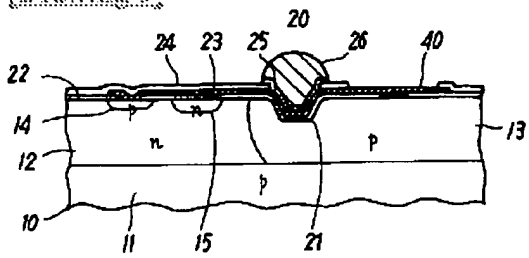
[Drawing 5]



[Drawing 2]



[Drawing 3]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平5－121409

(43)公開日　平成５年(1993)５月18日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/321				
		9168－4M	Ｈ０１Ｌ　21/ 92	C
		9168－4M		F

審査請求　未請求　請求項の数３(全　５　頁)

(21)出願番号　特願平3－283367

(22)出願日　平成３年(1991)10月30日

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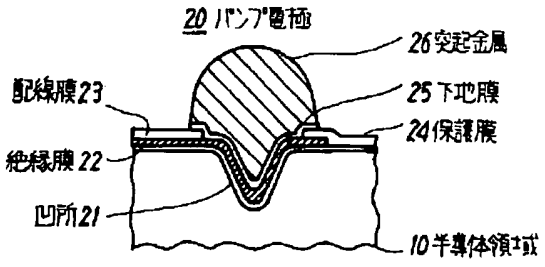
(54)【発明の名称】　集積回路装置用バンプ電極

(57)【要約】　（修正有）
【目的】集積回路装置用フリップチップに突設するバンプ電極を小形化した場合のチップへの取り付け強度を向上する。
【構成】チップの半導体領域１０内にＶ字状の凹所２１を掘り込み、その表面を含め半導体領域を絶縁膜２２で覆い、その上に集積回路の配線膜２３を配設し、チップ表面を覆う保護膜２４に窓を開口して凹所２１と配線膜２３を露出させ、窓部を配線膜２３と接続された薄い金属の下地膜２５で覆い、その上にバンプ電極２０用の突起金属２６を電解めっきにより突設する。



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【特許請求の範囲】

【請求項１】バンプ電極の下側の半導体領域内にＶ字状に掘り込まれた凹所と、この凹所を含む半導体領域の表面を覆う絶縁膜と、絶縁膜上に配設され集積回路と接続された金属の配線膜と、バンプ電極を設けるべき配線膜の所定範囲と凹所のみを窓内に露出させて集積回路装置の表面を覆う保護膜と、この保護膜の窓部を覆い配線膜と接続するよう設けられた薄い金属の下地膜と、下地膜の上に電解めっきにより突設された突起金属とを備えてなることを特徴とする集積回路装置用バンプ電極。

【請求項２】請求項１に記載のバンプ電極において、凹所の深さが開口幅と同程度以上とされることを特徴とする集積回路装置用バンプ電極。

【請求項３】請求項１に記載のバンプ電極において、突起金属の根元の幅が30μｍ以下とされることを特徴とする集積回路装置用バンプ電極。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は集積回路装置を外部と接続するためそのチップ上に突設される小形のバンプ電極ないしは突起電極に関する。

【０００２】

【従来の技術】近年の半導体集積回路装置の高集積化技術の著しい進展とともに、それを種々の電子回路や電子装置に組み込む際の実装形態の合理化，特に実装に要する手間の節減とスペースの縮小とが要求されるようになって来たが、周知のように集積回路装置のチップをプラスチックパッケージ等に一旦収納した上で実装するよりチップ状態のままで実装するのが有利であり、このため量産される電子装置類に上述のバンプ電極を突設させたいわゆるフリップチップが広く採用されるようになって来た。よく知られていることであるが、このバンプ電極の従来の代表的な構造を図５を参照して以下に簡単に説明する。

【０００３】図５は集積回路装置のチップの半導体領域10上にはんだのバンプ電極20が突設された状態を断面で示す。半導体領域10の表面を覆う酸化シリコン等の絶縁膜22の上側に半導体領域10内に作り込まれた集積回路と接続されたアルミの配線膜23が配設されており、その端部上にバンプ電極20を設けるため配線膜23を覆う窒化シリコン等の保護膜24に窓を開口して配線膜23を露出させる。この窓部をチタンや銅からなるごく薄い金属の下地膜25によりまず覆った後に、突起金属26を電解めっき法により所定の高さに成長させ、この例では短時間加熱により突起金属26のはんだを溶融させて先端に丸みを持つバンプ電極20とする。

【０００４】かかるバンプ電極20を備えるフリップチップの実装に当たっては、例えば図５とは逆に表面を下側に向けた姿勢で実装相手方の上に置き、バンプ電極20の先端を相手方の導体に接触させた状態で加熱して突起金

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属26のはんだを導体にはんだ付け接合する。これによってフリップチップの実装相手方に対する固定と接続が同時に果たされるので、実装作業に要する手間を省きかつ実装スペースを最小に縮小することができる。

【０００５】

【発明が解決しようとする課題】ところで、高集積化の進展により集積回路装置のチップサイズが縮小されるとともにチップ内に組み込まれる回路数も増加して外部接続点数が増加する傾向にあり、ある種の集積回路装置では数百個のバンプ電極を数㎜角のチップ内に配列する必要が出て来た。このため従来は 100μｍ程度の径ないし角であったバンプ電極のサイズを30μｍ以下にする必要があるが、小形化すると根元のチップへの取り付けないしは接合強度が低下する問題がある。

【０００６】すなわち、 100μｍ径のバンプ電極を30μｍにすると付け根の面積が約10分の１になりそれだけで強度が１桁低下するほか、図５の突起金属20と半導体領域10の間にある膜の相互密着性の信頼度が低下するため実際の接合強度がさらに低下して実装時等に掛かる僅かな外力により簡単に剥離しやすくなる。

【０００７】このようにバンプ電極の付け根の強度の強化が外部接続数の多い集積回路装置の高集積化のため必要な事情から、本発明はバンプ電極の半導体チップへの取り付け強度を高めることを目的とするものである。

【０００８】

【課題を解決するための手段】本発明によるバンプ電極では、その下側の半導体領域内に凹所をＶ字状に掘り込み、この凹所を含む半導体領域の表面を絶縁膜で覆い、絶縁膜上に集積回路と接続された金属の配線膜を配設し、配線膜の外部との接続個所と凹所のみを窓内に露出させて集積回路装置の表面を保護膜で覆い、この保護膜の窓部を配線膜と接続するように薄い金属の下地膜で覆い、下地膜の上に突起金属を電解めっきにより突設することによって上述の目的を達成する。

【０００９】なお、上述のＶ字状の凹所の深さはその開口幅と同程度以上とするのがバンプ電極の取り付け強度を高める上で望ましい。この凹所の開口面積はバンプ電極の根元の面積の25％以上とすることでふつうは取り付け強度を高める充分な効果が得られる。また、バンプ電極がとくに小形の場合は凹所内の配線膜を省いた構造とするのが有利である。かかる本発明によるバンプ電極はその付け根幅が前述のように30μｍ以下の場合に適用するのがとくに有利である。

【００１０】

【作用】本発明は、従来のバンプ電極の突起金属の半導体領域に対する取り付け強度が両者間にある膜の平坦面における密着性に頼っているため、外力をとくに横方向に受けた時この平坦な密着面にもっぱら剥離力が働く点に問題の原因があることに着目したもので、前項の構成にいうように半導体領域内にＶ字状に掘り込んだ凹所の

上に突起金属を突設することにより、突起金属に横方向の外力が掛かった時にその下側の膜や膜相互間に剥離力のほか必ず圧縮力が掛かるようにし、かつ密着面ないし外力の受容面の面積を凹所により広げることにより、バンプ電極の付け根の強度を従来より1桁以上高めることに成功したものである。

【0011】すなわち、横方向外力により突起金属に掛かる回転モーメント力に対して主に上述の圧縮力がその反力として働いて剥離力による反力はごく僅かで済むので、本発明のバンプ電極ではその付け根の剥離に対する強度を大幅に向上することができる。また、突起金属にはフリップチップの実装時に縦方向の圧力がもちろん掛かるが、上述のようにそれに対する受容面の面積が凹所により広がるのでこの縦方向外力に対するバンプ電極の付け根の強度も従来より向上する。

【0012】

【実施例】以下、図を参照して本発明の実施例を説明する。図1は本発明のバンプ電極の実施例の従来の図5に対応する断面図、図2はその製造方法を例示する断面図、図3はその適用例を示す集積回路装置のチップの要部拡大断面図、図4は本発明のバンプ電極の異なる実施例の断面図で、これらの図5に対応する部分に同符号が付されているので重複部分の説明は適宜省略することとする。

【0013】図1の実施例ではバンプ電極20の突起金属26にはんだが用いられ、そのサイズは例えば付け根で25～30μm径ないし角に，高さが20～25μmとされる。従来の図5と異なる点は半導体領域10内に凹所21が図示のようにV字状に掘り込まれ、その上にバンプ電極20の突起金属26が突設されていることである。この凹所21はその上部の開口の面積を突起金属60の付け根面積の25%以上に，その深さを開口の径ないしは幅と同程度か若干大きいめに掘り込むのがよく、例えばこの実施例では上部開口が15～20μm径ないし角，深さが15～25μmとされる。

【0014】この凹所21を除くバンプ電極20の構造は従来と同様であって、半導体領域10の表面は凹所21の表面を含めて絶縁膜22により覆われ、その上に金属の配線膜23が図示の例では凹所21内を含めて配設され、さらにその上に保護膜24が被着されてバンプ電極20を設けるべき範囲に配線膜23を露出させるように窓が開口される。薄い金属の下地膜25がこの窓内で配線膜23と接続するように設けられ、その上にはんだの突起金属26が電解めっきにより突設される。

【0015】ついで図2を参照して図1の構造のバンプ電極20を作り込む要領を説明する。図2(a)は半導体領域10の表面から凹所21を掘り込んだ状態を示す。この凹所21の掘り込みにはプラズマエッチング法やリアクティブイオンエッチング法を利用するのがよく、反応ガスとして例えば酸素を含む CF_4 と SF_6 の混合ガスを用い、ガス圧力とプラズマ電力を異方性エッチング条件に設定することにより凹所21を強い傾斜の正確なV字状の側面形状で深く掘り込むことができる。なお、かかる凹所21の掘り込みは半導体領域10に集積回路を作り込む前にあらかじめ行なって置くのが望ましい。

【0016】図2(b)では、まず半導体領域1の表面にふつうは酸化シリコンの絶縁膜22を例えば1～1.5 μm膜厚で付け、その表面上に 0.5～1.5 μmの膜厚のアルミの配線膜23を所定の配線パターンで配設する。ついで窒化シリコン等の保護膜24を1～2μmの膜厚にCVD法により成膜し、ドライエッチング法により窓24aをこれに開口して凹所21内を含む配線膜23の端部を露出させて図示の状態とする。図2(c)は下地膜25を全面に成膜した状態を示す。通例のようにこの下地膜25は2層膜とされ、この実施例では下側下地膜25aとしてチタンが0.2～0.5 μmの膜厚に，上側下地膜25bとして銅が1～1.5 μmの膜厚にそれぞれスパッタ法によって成膜される。

【0017】図に(d)は突起金属26を電解めっきにより突設した状態を示す。まず下地膜25の上側下地膜25bの方をフォトエッチングにより突起金属26用にパターンニングした後に、フォトレジスト膜30をスピンコートしてフォトプロセスによって上側下地膜25bのみを露出させる窓を明け、このフォトレジスト膜30をマスク膜とし下側下地膜25aを負側のめっき電極膜とする電解めっきにより突起金属26を図示のように上側下地膜25b上に選択的に成長させる。以降はフォトレジスト膜30を除去し、下側下地膜25aをエッチングにより上側下地膜25bの下側部分を除いて除去し、かつ前述のように短時間加熱によって突起金属26を溶融することによりその先端に丸みを持たせて図1に示す状態とする。

【0018】このようにして集積回路装置のチップに突設される図1の構造のバンプ電極20では、小形の場合でも縦横両方向に掛かる外力に対する付け根の強度が従来より前述のように1桁以上高く、チップの輸送時や実装時に受けやすい圧力や衝撃により剥離したり損傷を受けたりするトラブルを格段に減少させることができる。また、図2(d)の電解めっき工程後において下側下地膜25aのエッチング残渣を100Kg／cm^2 の高圧のジェット水流によって除去する実験の結果では、かなりの圧力が突起金属26に横方向に掛かったにも拘わらず、バンプ電極20の剥離はほぼ皆無であることが実証されている。

【0019】図3に図1のバンプ電極20を集積回路装置に組み込んだ適用例をその一部拡大断面で示す。この適用例でのウエハの半導体領域10は、p形の基板11の上にエピタキシャル層12をn形で成長させ、バンプ電極20を設けるべき各チップの周縁部にp形の接合分離層13を拡散したもので、エピタキシャル層12の表面部には集積回路用のp形層14やn形層15が図のように拡散され、絶縁膜22の上に配設された配線膜23はp形層14と接続されて

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いる。この配線膜23と接続するバンプ電極20は図の前後方向にできるだけ狭いピッチで配列できるよう図1で述べた30μm程度の狭い付け根幅にされるが、この適用例では電流容量を高めるため図の左右方向には例えば60μmの広い付け根幅に形成され、このため凹所21も図の左右方向にやや細長い矩形断面のV字状に掘り込まれる。

【0020】なお、集積回路装置は通例のようにウエハプロセスの終了後に試験されるが、バンプ電極20を本発明により50μm径程度以下に小形化すると試験用プローブのニードルを接触させるのが困難になるため、この図3の適用例ではバンプ電極20と接続された試験用の接続パッド40が設けられる。この接続パッド40は、例えばウエハをチップに単離する際にスクライブするためのいわゆるスクライブゾーンの面積を利用して、バンプ電極20よりかなり大きいめの例えば80μm角のサイズで作り込まれる。このため配線膜23の端部を膨出させ、保護膜24に明けた窓内にこれを露出させて接続パッド40とする。

【0021】図4に突起金属26に例えば金や銅を用いる小電流容量のバンプ電極20を図1の場合よりもさらに小形化するに適する実施例を断面で示す。このバンプ電極20の付け根の幅を例えば20μm程度にする場合は凹所21の開口幅が10～15μmになるので、この図4の実施例では凹所21内の配線膜23が省かれてその周辺にのみ配設されている。下地膜25はもちろんこの配線膜23と接続するようかつ凹所21内にも設けられ、その上に突起金属26用の金や銅が電解めっき法によって成長される。これによって突起金属26は凹所21内にいわば根をしっかりと下ろした形になり、半導体領域10に対する高い取り付け強度が得られる。なお、この実施例の場合の下地膜21中の上側下地膜にはパラジュウム等が用いられ、その膜厚は図1の場合より薄く 0.4～0.6 μm程度とするのがよい。この図3の実施例の構造はバンプ電極20を20μm程度以下のサイズにする場合に有利である。

【0022】

【発明の効果】以上のとおり本発明によるバンプ電極では、その下側の半導体領域内に凹所をV字状に掘り込み、この凹所を含む半導体領域の表面を絶縁膜で覆い、その上に集積回路と接続された金属の配線膜を配設し、その外部接続個所と凹所を窓内に露出させて集積回路装置の表面を保護膜で覆い、窓部を配線膜と接続するように薄い金属の下地膜で覆い、下地膜の上に突起金属を電

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解めっき法により突設するようにしたので、突起金属に外力がとくに横方向に掛かったときその下側の膜や膜相互間に剥離力のほかに必ず圧縮力が掛かり、かつ密着面ないし外力の受容面の面積が広がってバンプ電極の付け根強度が従来より1桁以上向上し、縦方向の外力に対しても受容面の面積が広がる分だけ付け根強度が向上する。

【0023】本発明は外部接続点数の多いフリップチップ用の小形のバンプ電極に適用してとくに効果が高く、従来から高集積化上の隘路であったバンプ電極のチップへの取り付け強度を高めて付け根のサイズを30μm以下に縮小することを可能にし、数mm角の小形チップに数百個のバンプ電極を配列した集積度の高い集積回路装置の提供を可能にするものである。

【図面の簡単な説明】

【図1】本発明のバンプ電極の実施例の断面図である。

【図2】図1のバンプ電極の製造方法を例示する断面図であり、同図(a)は凹所の掘り込み後の状態，同図(b)は下地膜の被着前の状態，同図(c)は下地膜の被着後の状態，同図(d)は突起金属の電解めっき後の状態をそれぞれ示す。

【図3】図1のバンプ電極の集積回路装置への適用例を示すフリップチップの要部拡大断面図である。

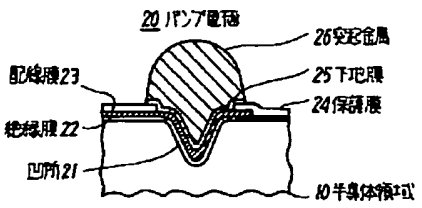
【図4】本発明のバンプ電極の異なる実施例の断面図である。

【図5】従来のバンプ電極の断面図である。

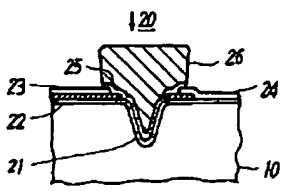
【符号の説明】

10	集積回路装置のチップないしウエハの半導体領域
20	バンプ電極
21	凹所
22	絶縁膜
23	配線膜
24	保護膜
25	下地膜
25a	下側下地膜
25b	上側下地膜
26	突起金属
30	電解めっき用のマスクとしてのフォトレジスト膜

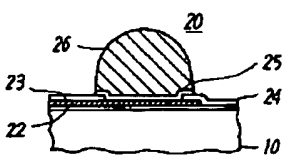
【図1】



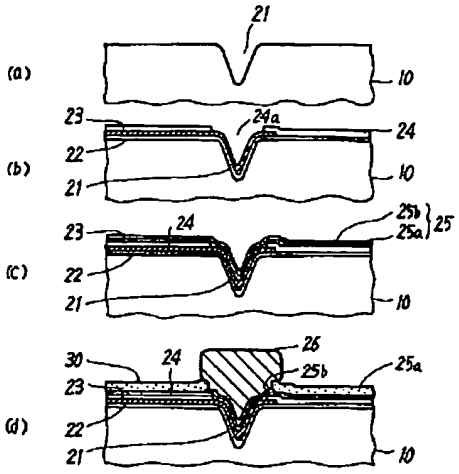
【図4】



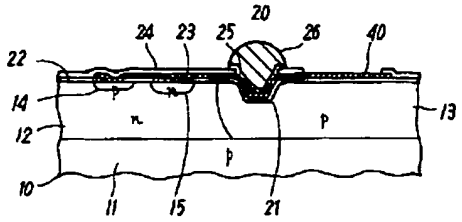
【図5】



【図2】


(a)
21
10
(b)
23
24a
24
22
21
10
(c)
23
24
25b
25a
25
22
21
10
(d)
30
24
26
25b
25a
23
22
21
10

【図3】


20
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21

PAT-NO: JP405121409A

DOCUMENT-IDENTIFIER: JP 05121409 A

TITLE: BUMP ELECTRODE FOR INTEGRATED CIRCUIT DEVICE

PUBN-DATE: May 18, 1993

INVENTOR-INFORMATION:
NAME
AMANO, AKIRA

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJI ELECTRIC CO LTD N/A

APPL-NO: JP03283367

APPL-DATE: October 30, 1991

INT-CL (IPC): H01L021/321

ABSTRACT:

PURPOSE: To increase attaching strength of a bump electrode which is bumped
and fixed to the flip chip for an integrated circuit device even if the bump electrode is miniaturized.

CONSTITUTION: A V-shape recess 21 is provided in a semiconductor area 10 of
a chip, and the semiconductor area including the surface is covered with an insulating film 22. On top of that a wiring film 23 of an integrated circuit is laid out. Then, a window is provided on a protecting film 24 covering a chip surface so as to expose the recess 21 and the wiring film 23. The window
part is coated with a thin metal base film 25 connected with the wiring film 23. On top of that, a projecting metal 26 for a bump electrode 20 is bumped and fixed by electroplating.